Lecture No 3

The Instruction Set

The Instruction Set

Instruction Sets define the many different kinds of data and their manipulations by different processors.

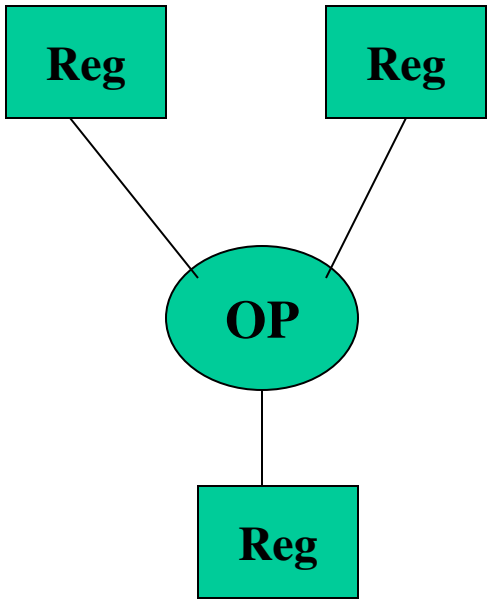
The major three *Instruction Set* Types are:

1. ***The L/S Architecture (Load-Store)***
2. ***The R/M Architecture (Register- Memory)***
3. ***The R+M Architecture (Register-plus-memory)***

The Instruction Set (Contd..)

The major three *Instruction Set* Types are:

The L/S Architecture: **The L/S or Load Store architecture specifies that all operand values must be loaded from Memory into Registers before an execution can take place.**



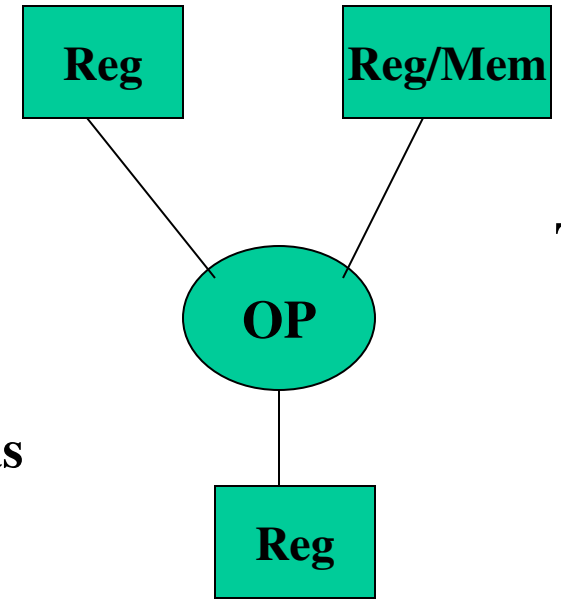
An ALU ADD instruction must have both *Operands* and *Result* specified as Registers (Three Address Format).

Operand in Memory is not allowed

Mostly used in RISC machines. RISC architecture tries to reduce the amount of complexity in the Instruction Set itself and regularize the instruction format so as to simplify decoding of Instructions.

The Instruction Set (Contd..)

The R/M Architecture: **The R/M or Register Memory architecture includes instructions that can operate both on registers and one operand in Memory.**



An ALU ADD instruction one source operand lies in Memory and the other source operand lies in Register which also serves as Destination

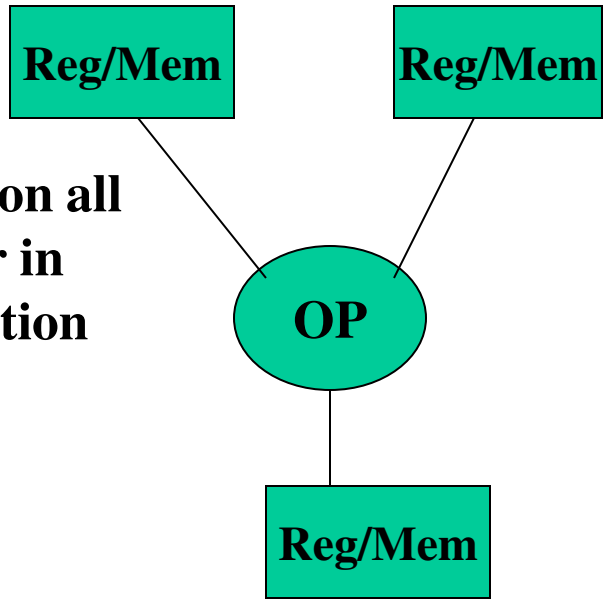
Two address Format

Most general purpose modern mainframe computers like IBM, Hitachi, Fujitsu etc as well as several microprocessors (Intel X86 Series) follow R/M Style.

The Instruction Set (Contd..)

The R+M Architecture: **The R+M or Register Plus Memory architecture includes instructions that can operate on operands both in registers and Memory.**

In an ALU ADD instruction all operand lie in Memory or in Registers or any combination there off.



Two address Format

(One source operand in Register or Memory is also the Destination)

Three address Format

(Three operands independently specified and each may be a register or Memory

Digital Equipments (DEC) VAX series of machines And Motorola M680X0 series of microprocessors use this architecture.